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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/007,555	11/08/2001	Hung T. Nguyen	01-623	4891

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EXAMINER
AUVE, GLENN ALLEN

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 09/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/007,555	NGUYEN ET AL.	
	Examiner	Art Unit	
	Glenn A. Auve	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-11,15-19,23* is/are rejected.

7)☒ Claim(s) *4-6,12-14 and 20-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3,7-11,15-19 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamashita et al., U.S. Pat. No. 6,516,378 B1.

As per claim 1, Yamashita et al. (Yamashita) shows a processor having separate instruction (IB) and data (DB) buses, separate instruction (41) and data (42) memories, and separate instruction (51,52) and data (53) units, a mechanism supporting self-modifying code comprising a crosstie bus coupling the instruction bus and data unit (see the path as shown in figs. 12M,N, and O); and a request arbiter coupled between the instruction and data units, that arbitrates requests therefrom for access to the instruction memory (fig.3,81). Yamashita shows all of the elements recited in claim 1.

As for claim 2, the argument for claim 1 applies. Yamashita also shows that the data unit can employ the instruction memory to contain data (col.16, and inherent in that any memory can be broadly interpreted to contain "data" of some sort). Yamashita shows all of the elements recited in claim 2.

As for claim 3, the argument for claim 1 applies. Yamashita also shows that the request arbiter gives higher priority to requests from the data unit (col.14, lines 26-35). Yamashita shows all of the elements recited in claim 3.

As for claim 7, the argument for claim 1 applies. Yamashita also shows that the instruction memory is local and the processor further comprises an external memory interface (e.g. 62). Yamashita shows all of the elements recited in claim 7.

As for claim 8, the argument for claim 1 applies. Yamashita also shows that the processor is a digital signal processor (inherent in that the processor processes digital signals). Yamashita shows all of the elements recited in claim 8.

As per claim 9, Yamashita shows a method of supporting self-modifying code in a processor having separate instruction (IB) and data (DB) buses, separate instruction (41) and data (42) memories, and separate instruction (51,52) and data (53) units, comprising arbitrating requests from the instruction and data units for access to the instruction memory (operation of arbiter 81); and communicating instructions between the instruction bus and data unit via a crosstie bus therebetween (see cols.14 and 16 and the path as shown in figs. 12M,N, and O). Yamashita shows all of the steps recited in claim 9.

As for claim 10, the argument for claim 9 applies. Yamashita also shows that the data unit can employ the instruction memory to contain data (col.16, and inherent in that any memory can be broadly interpreted to contain "data" of some sort). Yamashita shows all of the elements recited in claim 10.

As for claim 11, the argument for claim 9 applies. Yamashita also shows that the request arbiter gives higher priority to requests from the data unit (col.14, lines 26-35). Yamashita shows all of the elements recited in claim 3.

As for claim 15, the argument for claim 9 applies. Yamashita also shows that the instruction memory is local and the processor further comprises an external memory interface (e.g. 62). Yamashita shows all of the elements recited in claim 15.

As for claim 16, the argument for claim 9 applies. Yamashita also shows that the processor is a digital signal processor (inherent in that the processor processes digital signals). Yamashita shows all of the elements recited in claim 16.

As per claim 17, Yamashita et al. (Yamashita) shows a digital signal processor comprising an execution core (20) having an instruction cache; a memory unit coupled to the core and having separate instruction (IB) and data (DB) buses, separate instruction (41) and data (42) memories, and separate instruction (51,52) and data (53) units; a crosstie bus coupling the instruction bus and data unit (see the path as shown in figs. 12M,N, and O); and a request arbiter coupled between the instruction and data units, that arbitrates requests therefrom for access to the instruction memory (fig.3,81). Yamashita shows all of the elements recited in claim 17.

As for claim 18, the argument for claim 17 applies. Yamashita also shows that the data unit can employ the instruction memory to contain data (col.16, and inherent in that any memory can be broadly interpreted to contain "data" of some sort). Yamashita shows all of the elements recited in claim 18.

As for claim 19, the argument for claim 17 applies. Yamashita also shows that the request arbiter gives higher priority to requests from the data unit (col.14, lines 26-35). Yamashita shows all of the elements recited in claim 19.

As for claim 23, the argument for claim 17 applies. Yamashita also shows that the instruction memory is local and the processor further comprises an external memory interface (e.g. 62). Yamashita shows all of the elements recited in claim 23.

Allowable Subject Matter

3. Claims 4-6,12-14, and 20-22 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is a statement of reasons for the indication of allowable subject matter: With respect to claims 4,12, and 20, the prior art does not show the combination of a prefetch mechanism and the request arbiter stalling the prefetch mechanism when the arbiter grants a request from the data unit for access to the instruction memory.

Response to Arguments

5. Applicant's arguments filed July 23, 2004, have been fully considered but they are not persuasive. Applicant argues that Yamashita does not teach separate data and instruction units. However, the examiner has pointed out above that the "instruction unit" is denoted by element 51 or 52 in Yamashita and the data unit is denoted by element 53. These are separate units. Therefore this argument is not persuasive.

6. Applicant also argues that the elements 51 and 52 have no control functionality and as such they cannot be construed as the instruction units. However there is no limitation in the claims requiring that the "instruction unit" has any sort of control functionality. The program RAM (52) and ROM (51) hold instructions and as such they can be construed as "instruction units". Therefore this argument is not persuasive.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn A. Auve whose telephone number is (703) 305-9638. After October 13, 2004, the examiner's telephone number will change to (571) 272-3623. The examiner can normally be reached on M-Th 8:00 AM-5:30 PM, every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Glenn A. Auve
Primary Examiner
Art Unit 2111

gaa
September 7, 2004